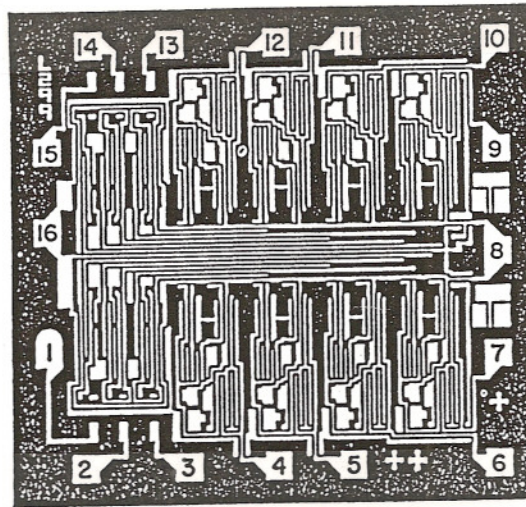




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



<u>Pad</u>	<u>Function</u>	<u>Pad</u>	<u>Function</u>
1	E	9	Q3
2	A	10	Q2
3	B	11	Q1
4	Q0	12	Q0
5	Q1	13	B
6	Q2	14	A
7	Q3	15	E
8	VSS	16	VDD

**Topside Metal: Al**

**Backside: Si**

**Backside Potential: VDD**

**Mask Ref: 6627**

**Bond Pads (Mils): 2S**

**APPROVED BY:**

**MFG: Harris**

**DIE SIZE (Mils): 83 X 79 X 20**

**THICKNESS:**

**DATE: 3/13/00**

**P/N: CD4555B**

DG 10.1.2  
 Rev A 3-4-99